CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1 – 25. (canceled)

26. (currently amended) A programmable logic device comprising:

a plurality of resources logically subdivided into a plurality of programmable logic blocks;

a first voltage supply terminal configured to receive a first supply voltage;

~~and~~

a plurality of first switch elements, wherein each first switch element is coupled between one of the programmable logic blocks and the first voltage supply terminal; and

a control circuit coupled to the plurality of first switch elements,

wherein the control circuit is configured to provide a plurality of control signals for controlling the plurality of first switch elements,

wherein the control circuit comprises a plurality of configuration memory cells configured to store a corresponding plurality of configuration data values, wherein the control circuit provides the plurality of control signals in response to the plurality of configuration data values, and

wherein the plurality of configuration data values identify unused programmable logic blocks determined at design time.

27. (original) The programmable logic device of Claim 26, further comprising:

a second voltage supply terminal configured to receive a second supply voltage; and

a plurality of second switch elements, wherein each second switch element is coupled between one of the programmable logic blocks and the second voltage supply terminal.

28.-29. (canceled)

30. (currently amended) The programmable logic device of Claim ~~29~~ 26, wherein the control circuit further comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit further provides the plurality of control signals in response to the plurality of user control signals.

31. (canceled)

32. (original) The programmable logic device of Claim 26, wherein each first switch element comprises a transistor.

33. (withdrawn) A programmable logic device comprising:

a first voltage supply terminal configured to receive a first supply voltage;

a plurality of programmable logic blocks, each programmable logic block comprising one or more resources of the programmable logic device; and

a plurality of voltage regulators, wherein each voltage regulator is coupled between one of the programmable logic blocks and the first voltage supply terminal.

34. (withdrawn) The programmable logic device of Claim 33, further comprising a control circuit coupled to each of the voltage regulators, wherein the control circuit is configured to provide a plurality of control signals for controlling the plurality of voltage regulators.

35. (withdrawn) The programmable logic device of Claim 34, wherein the control circuit comprises a plurality of configuration memory cells configured to store a corresponding plurality of configuration data values, wherein the control circuit provides the plurality of control signals in response to the plurality of configuration data values.

36. (withdrawn) The programmable logic device of Claim 35, wherein the control circuit further comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit further provides the plurality of control signals in response to the plurality of user control signals.

37. (withdrawn) The programmable logic device of Claim 34, wherein the control circuit comprises a plurality of user control terminals configured to receive a corresponding plurality of user control signals, wherein the control circuit provides the plurality of control signals in response to the plurality of user control signals.

38. (new) The programmable logic device of Claim 26, wherein the plurality of configuration data values stored in the plurality of configuration memory cells is part of a configuration bit stream provided for configuring the programmable logic device.

39. (new) The programmable logic device of Claim 30, wherein the plurality of user control signals identify inactive programmable logic blocks.

40. (new) The programmable logic device of Claim 39, wherein the inactive programmable logic blocks are determined at run time.